

# 8051 microcontroller

## Chapter One--- Introduction

1. When comparing a system board based on a microcontrollers and general-purpose microprocessor, which one is cheaper?
2. A microcontroller normally has which of the following devices on-chip?
  - (a) RAM
  - (b) ROM
  - (c) I/O
  - (d) all of the above
3. Consider the following human interface devices: a joystick, a light pen, a mouse, a microphone, and a loudspeaker. Which are input devices? Which are output devices?
4. Comparing a microcontroller-based system to a microprocessor-based system, which is more likely to rely on? Why?
5. What is the difference between a microprocessor and a Microcontroller?
6. Why it is not possible to protect a microprocessor-based system from software piracy?
7. What are the advantages of a microcontroller over a microprocessor?
8. What are the advantages and disadvantages of Princeton (Von Neumann) Architecture against Harvard Architecture?
9. In spite of offering on-chip program an data memory, why additional external memory interfacing provision is available in microcontrollers?
10. The type of program memory available in 87XX series of microcontrollers is \_\_\_\_\_.
  - (a) EPROM
  - (b) FLASH
  - (c) OTP
  - (d) None of these
11. 'Sleep' and 'idle' modes are offered in microcontrollers for \_\_\_\_\_.
  - (a) serial communications
  - (b) memory management
  - (c) I/O configuration
  - (d) None of these

## Chapter Two---Architecture of 8051

1. What is the major difference between port 0 and the other three ports of XX51?
2. What is the purpose of the ALE signal?
3. What is locked by program lock bits? What is the purpose of providing this?
4. How should the following on-chip data memory locations be addressed?
  - (a) Lower 128 bytes from 00H to 7FH.
  - (b) Upper 128 bytes from 80H to FFH.

- (c) Special function registers located within 80H to FFH.
5. At any time how many general-purpose registers located between 00H and 1FH of XX51 may be used? Why R0 and R1 are different from the remaining registers?
  6. If bit 0 is taken as LSB and bit 7 as the MSB, then what would be the bit-address of bit 3 of internal data memory location 29H?
  7. In general, a 12MHz crystal is used for 8051-based systems. However, in certain cases, a frequency of 11.0592 is preferred. What is the reason behind it?
  8. What is the relation between machine cycle, state and pulse for any XX51 microcontroller?
  9. Why is it important to study the reset initialization details of any microcontroller? Are the internal RAM locations cleared by a system reset?
  10. What is the maximum total size of data memory, which may be directly addressed by the 8752 microcontroller? What type of address bus makes it possible?
  11. What is the width (number of bits) of the address bus for internal data memory of XX52?
  12. Upon power-up, the 8051 fetches the first opcode from ROM address location \_\_\_\_\_.
  13. Which 8051 port needs pull-up resistors to function as an I/O port?
  14. How many SFRs are there in 8051?
    - (a) 20
    - (b) 21
    - (c) 27
    - (d) none of these
  15. What should be the values of RS1 and RS0 bits of PSW SFR to select register bank #2?
    - (a) 1 and 0, respectively
    - (b) 1 and 1
    - (c) 0 and 0
    - (d) none of these
  16. How would you address bit 3(bit 0 being LSB) of accumulator?
    - (a) ACC.3
    - (b) E3H
    - (c) Either of these
    - (d) none of these
  17. What is the special function of register B?
    - (a)Substitute accumulator
    - (b) To perform 16-bit operations along with accumulator
    - (c) Serve as a pointer register
    - (d) none of these
  18. What is the value of accumulator after system reset?
    - (a) XXH
    - (b) FFH
    - (c) 00H
    - (d) none of these
  19. Which register bank is selected by default after system reset?
    - (a) #0

- (b) #1
  - (c) #2
  - (d) none of these
20. What is the reset value of the SP?
- (a) 00H
  - (b) 07H
  - (c) FFH
  - (d) none of these
21. If we write 0 in the output latch of a port bit before reading it, then at the time of reading that port pin, we would always read it as \_\_\_\_.
- (a) 0
  - (b) 1
  - (c) Undefined
  - (d) none of these
22. Which of the following ports of MCS-51 might be designated as a true bi-directional port?
- (a) port 2
  - (b) port 1
  - (c) port 0
  - (d) none of these
23. At output, all ports of MCS-51 have
- (a) Internal transistor pull-ups
  - (b) Internal FET pull-ups
  - (c) Internal resistance pull-ups
  - (d) none of these
24. The size of on-chip program memory for 8051 is \_\_\_\_.
- (a) 4K bytes
  - (b) 8K bytes
  - (c) 16K bytes
  - (d) none of these
25. The size of on-chip data memory for 8051 is \_\_\_\_.
- (a) 64 bytes
  - (b) 128 bytes
  - (c) 256 bytes
  - (d) none of these
26. One machine cycle of 8051 takes \_\_\_\_.
- (a) 12 clock pulses
  - (b) 6 states
  - (c) Both of these
  - (d) none of these
27. Reset input of 8051 should remain high for \_\_\_\_.
- (a) 1 machine cycle
  - (b) 2 states
  - (c) 3 clock periods
  - (d) none of these

28. Reset input for 8051 \_\_\_\_.
- (a) clears all ports
  - (b) loads SP by 00H
  - (c) selects bank #1
  - (d) none of these
29. Give the size of RAM in each of the following.
- (a) 8051      (b) 8052      (c) 8031
30. Give the size of the on-chip ROM in each of the following.
- (a) 8051      (b) 8052      (c) 8031
31. Apart from the accumulator, is there any other register involved in multiply and division instructions' execution?
32. What is the purpose of port registers?
33. What is the difference between CY and OV flags of PSW?
34. If the SP is loaded with 23H, from which address would the system stack grow?
35. Why was it necessary to provide two reading buffers in the ports of MCS-51?
36. Can the memory area unoccupied by SFRs be used as general-purpose storage area?

## Chapter Three--- Instruction set

1. What is the addressing mode of the instruction MOV R0, #03H?
- (a) Immediate
  - (b) Register direct
  - (c) Register indirect
  - (d) None of these
2. What type of instruction is 'POP'?
- (a) Arithmetic
  - (b) Program branching
  - (c) Logical operation
  - (d) None of these
3. What would happen if the following instruction is executed?
- MOV PSW, #18H
- (a) R0 of bank #3 would be copied to PSW register
  - (b) Bank #3 would be selected
  - (c) Content of the location whose address is in R0 of bank #3 would be copied to PSW
  - (d) None of these
4. Assuming that bank #0 is selected and register R0 of this bank contains 80H, which of the following instructions would copy the data from port 0 to register B?
- (a) MOV 0F0H, 80H
  - (b) MOV B, @R0
  - (c) MOV F0H, @R0
  - (d) None of these
5. Assuming that bank #2 is selected and register R0 of bank #2 contains E0H and register R1 of

bank #2 contains 15H, which of the following instructions would not copy the data from location E0H to location 15H?

- (a) MOV R5, A
- (b) MOV @R1, 0E0H
- (c) MOV 15H, @R0
- (d) None of these

6. What would be the content of DPH after execution of MOV DPTR, #1234H instruction?

- (a) 12H
- (b) 34H
- (c) 1234H
- (d) None of these

7. What would be the content of the accumulator after execution of the instruction, MOV A, SP just after system reset?

- (a) Undefined
- (b) 07H
- (c) 08H
- (d) None of these

8. What is meant by 'Addressing Mode'? How many addressing modes are there in MCS-51? Give one example of each type.

9. What is the difference between MOVC and MOVX instructions?

10. Which part of the internal RAM is related with PUSH and POP instructions?

11. What is the difference between XCH and XCHD instructions?

12. Match the following instructions, in the left column, with the addressing modes on the right.

Instruction	Addressing mode
MOV P2, #0FH	Register direct
MOV P0, P2	Register indirect
MOV A, R5	Immediate
MOV A, @R0	Direct
MOV @R0, 0F0H	Immediate
MOV R0, #22H	Register direct
MOV 0FFH, @R1	Direct
MOV B, R7	Register indirect

13.(a) Does the MOV instruction read from the port pins or the output latch?

(b) Does the MOV instruction write in the port pins or the output latch?

14. What would happen if the # symbol is removed from a data in an MOV instruction?

15. What happens to the source location after its content is copied to a destination location using MOV instruction?

16. Which instruction would you use to select register bank #2?

17. Write a program for storing the current value in accumulator at location 23H and then storing the input data from port 0 in the accumulator?

18. write a program to exchange the data between R0 and R1 of the current register bank?

19. What would be the result if 0110 0010B is added with 0001 0001B using ADDC instruction and the CY flag was cleared before the execution of the instruction?

- (a) 0111 0100B
  - (b) 0111 0011B
  - (c) 1000 0110B
  - (d) None of these
20. Which of the following instructions would clear the CY flag?
- (a) CLR PSW
  - (b) CLR ALL
  - (c) MOV PSW, #00H
  - (d) None of these
21. What would be the content of register R7 after execution of INC R7 instruction, if initially it contained 2FH?
- (a) 3FH
  - (b) 2FH
  - (c) 20H
  - (d) None of these
22. What would be the content of DPTR after execution of INC DPTR instruction, if initially it contained F0FFH?
- (a) 00FFH
  - (b) F000H
  - (c) F100H
  - (d) None of these
23. If 3DH in accumulator is added with F1H in register B using ADDC instruction and the CY flag was set before the execution of the instruction then which of the following flags would not be set?
- (a) OV and AC flags
  - (b) CY and AC flags
  - (c) P and OV flags
  - (d) None of these
24. Which of the following flags would be set when R2, originally having 00H, is decremented by one using the instruction DEC R2?
- (a) AC flag
  - (b) CY flag
  - (c) OV flag
  - (d) None of these
25. Assuming the CY flag is set (1) and accumulator contains 00H, what would be the content of accumulator after executing SUBB A, #00H following by ADD A, #00H?
- (a) 00H
  - (b) 01H
  - (c) FFH
  - (d) None of these
26. Assuming accumulator contains 01H, CY flag is 0 and data memory location 30H contains FFH, which of the following instructions, when executed, would set the CY flag?
- (a) INC 30H
  - (b) ADD A, 30H

- (c) DEC A
  - (d) None of these
27. What would be the content of the accumulator when the following program is executed?
- ```
MOV PSW, #00H
MOV R4, A
SUBB A, R4
```
- (a) Undefined
  - (b) 00H
  - (c) 01H
  - (d) None of these
28. What is the difference between ADD and ADDC instructions?
29. What is the purpose of the CY flag?
30. What precaution should we take before using SUBB instruction?
31. Which of the following two instructions would be more appropriate to increment the accumulator by one? INC A or ADD A, #01H? Justify your answer.
32. Why is there no provision of 'DEC DPTR' instruction in MCS-51?
33. Is it possible to subtract the content of a register from the accumulator without using SUBB instruction?
34. After executing the following program, the accumulator contained 00H. What was the initial content of register R2?
- ```
MOV A, R2
ADDC A, R2
INC A
```
35. What is the limit of LJMP instruction?
- (a) 256 bytes
  - (b) 2K bytes
  - (c) 64K bytes
  - (d) None of these
36. How many bits of the jumping address are available in AJMP instruction?
- (a) 11 bits
  - (b) 10 bits
  - (c) 9 bits
  - (d) None of these
37. The second byte of the SJMP instruction indicates the displacement in\_\_\_\_\_.
- (a) signed magnitude form
  - (b) two's complement form
  - (c) either one of the above
  - (d) None of these
38. JZ instruction is applicable
- (a) only for registers
  - (b) only for SFRs
  - (c) only for register A
  - (d) None of these
39. How many flags of PSW are affected by CJNE instruction?

- (a) None
  - (b) Only carry flag
  - (c) All four flags
  - (d) None of these
40. What is the common point between JZ, JNZ, CJNE and DJNZ instructions?
- (a) All are 3-byte instructions
  - (b) All use displacement bytes for branching
  - (c) All depend on the Z-flag's status
  - (d) None of these
41. If register R7 contains 00H before execution of the instruction DJNZ R7, 02H, from which address would the next instruction after it be executed? Assume that the DJNZ instruction is located at 005FH.
- (a) 005FH
  - (b) 0061H
  - (c) 0063H
  - (d) None of these
42. Which of the following instructions affects any flag of PSW?
- (a) SJMP
  - (b) DJNZ
  - (c) NOP
  - (d) None of these
43. What would the processor do after executing the instruction SJMP 0FEH?
- (a) Execute from 0FEH
  - (b) Execute the same instruction again
  - (c) Execute from 0002H
  - (d) None of these
44. What is the purpose of NOP instruction?
45. Both SJMP and AJMP are of 2 bytes and take two cycles to be executed. Why two different mnemonics are provided for the same purpose?
46. From which address would the next executable instruction be fetched by the LCALL 0123H instruction, if the first byte of it is located at 0023H?
- (a) 0123H
  - (b) 2301H
  - (c) 0026H
  - (d) None of these
47. If the first byte of an ACALL instruction is located at 0123H and before its execution SP contained 23H, then what would be the content of the internal RAM location 24H immediately after execution of the ACALL instruction?
- (a) 01H
  - (b) 23H
  - (c) 25H
  - (d) None of these
48. How many flags are affected by the execution of the following instruction?
- POP 0D0H



- (a) No flags are affected
- (b) Only C flag is affected
- (c) All flags are affected
- (d) None of these

49. What would happen if the following subroutine is executed?

```
SUBRT0:  PUSH  A
          PUSH  B
          POP   A
          POP   B
          RET
```

- (a) Nothing happens
- (b) Data present in registers A and B are interchanged
- (c) Returns to the address by combining registers A and B
- (d) None of these

50. In a case of nested subroutines, main program calls subroutine 1, which calls subroutine 2. If subroutine 2 was developed as follows, what would happen after the execution of subroutine 2?

```
SUBRT2:  DEC     81H
          DEC     81H
          RET
```

- (a) Return to main program
- (b) Return to subroutine 1
- (c) Stack underflow
- (d) None of these

51. What is the main drawback of using subroutines?

- (a) Needs extra space
- (b) Needs extra time
- (c) Hampers program flow
- (d) None of these

52. What would be the content of the accumulator after execution of the following main program?

```
MAIN:    MOV    R7, #22H
          MOV    A, #00H
          LCALL LOAD33
          ADD   A, 1FH
OVER:    SJMP   OVER
LOAD33:  PUSH   PSW
          MOV   PSW, #18H
          MOV   R7, #33H
          POP   PSW
          RET
```

- (a) 1FH
- (b) 33H
- (c) 22H
- (d) None of these

53. What would happen when the following program is executed?

```

MAIN:    MOV    A, #01H
         MOV    B, #0FFH
         PUSH   B
         PUSH   A
         RET

```

- (a) It would jump at the program memory location 01FFH
  - (b) It would execute a call at location FF01H
  - (c) Undefined
  - (d) None of these
54. What would be the value of bit 7 (MSB) of the accumulator after execution of the following two instructions?
- ```

PUSH   PSW
POP    ACC

```
55. Is it possible to use the bit-addressable area of internal data memory for the purpose of stack?
56. The AND instruction is generally used to \_\_\_\_.
- (a) Set a few bits
  - (b) Clear a few bits
  - (c) Complement a few bits
  - (d) None of these
57. The OR instruction is generally used to \_\_\_\_.
- (a) Set a few bits
  - (b) Clear a few bits
  - (c) Complement a few bits
  - (d) None of these
58. The XOR instruction is generally used to \_\_\_\_.
- (a) Set a few bits
  - (b) Clear a few bits
  - (c) Complement a few bits
  - (d) None of these
59. Which of the following instructions, when executed, would leave the accumulator unchanged?
- (a) ANL A, #0FFH
  - (b) ORL A, #00H
  - (c) Either of these
  - (d) None of these
60. Execution of which one of the following instructions affects the Carry flag?
- (a) RR A
  - (b) CPL A
  - (c) CLR A
  - (d) None of these
61. Assuming that Carry flag is set, which of the following instructions, when executed, would double the accumulator content if its original content is less than 127d?
- (a) RL A
  - (b) RLC A
  - (c) RR A

- (d) None of these
62. Assuming accumulator contains 80H and the Carry flag is cleared, which of the following instructions, when executed, would set the Carry flag and clear the accumulator?
- (a) RRC A  
 (b) RLC A  
 (c) RL A  
 (d) None of these
63. Which of the following instructions, when executed four times, would interchange (swap) the nibbles of the accumulator?
- (a) RR A  
 (b) RL A  
 (c) Either of these  
 (d) None of these
64. Instead of using the instruction ANL A, #00H, which of the following instructions may be used to get the same effect?
- (a) CPL A  
 (b) CLR A  
 (c) Either of these  
 (d) None of these
65. Instead of using the instruction XRL A, #0FFH, which of the following instructions may be used to get the same effect?
- (a) CPL A  
 (b) CLR A  
 (c) Either of these  
 (d) None of these
66. What is the difference between XRL A, direct and XRL direct, A instructions?
67. What is the difference between RL A and RLC A instructions?
68. What is the easiest way to divide a number in the accumulator by 4?
69. Which bits of the accumulator would contain 0 after executing the following instruction?  
 ANL A, #88H
70. How many bits of the accumulator would be toggled after execution of the instruction XRL A, #0FFH?
71. What would be the content of bit 3 of the accumulator after execution of RL A instruction if the accumulator originally contained 29H?
72. Is it possible to implement NOR and NAND operations through MCS-51 instruction set? Justify your answer.
73. What would be the accumulator content after executing the following instruction?  
 START: CLR A  
 CPL A
74. What would be the accumulator content after execution of the XRL A, 0E0H instruction?
75. Which of the following two instructions may be used to find the input of bit 0 (LSB) of a port after reading the port and placing its value in the accumulator? Justify your answer.  
 RLC A            RRC A
76. What is the purpose of the following sub-routine?

```
START: MOV    R7, #04H
LOOP:  RL     A
      DJNZ   R7, LOOP
      RET
```

77. How can the XRL operation be implemented using any combination of ANL, ORL and CPL instructions?

78. Which flag of PSW is generally involved in Boolean variable manipulation?

- (a) AC
- (b) OV
- (c) P
- (d) None of these

79. Which set of the following instructions is a substitute for SETB C instruction?

- (a) CLRC  
CPL C
- (b) CPLC  
CLRC
- (c) CPL C  
CPL C
- (d) None of these

80. Which of the following instruction may substitute CLR C instruction?

- (a) CLR 0D0H
- (b) CLR 0D7H
- (c) CLR 0D8H
- (d) None of these

81. Which byte of the JNB instruction contains the bit address?

- (a) First
- (b) Second
- (c) Third
- (d) None of these

82. If a JB instruction is placed at the address 0200H and the addressed bit is not set, from which address the next instruction would be executed?

- (a) 01FFH
- (b) 0201H
- (c) 0203H
- (d) None of these

83. Which one of the following can perform a NAND operation?

- (a) CPL C following by ANL C, bit
- (b) ANL C, /bit
- (c) ANL C, bit following by CPL C
- (d) None of these

84. With respect to MOV C, bit instruction, MOV bit, C instruction takes

- (a) one cycle less
- (b) same cycle
- (c) one cycle more

- (d) None of these
85. In which of the following conditions ANL C, bit and ANL C, /bit instruction would produce identical results for the same values of C and addressed bit?
- If CY = 0
  - If CY = 1
  - If bit = 0
  - None of these
86. In which of the following conditions ORL C, bit and ORL C, /bit instruction would produce identical results for the same values of C and addressed bit?
- If CY = 0
  - If CY = 1
  - If bit = 0
  - None of these
87. Which of the following instructions may replace JNC instruction?
- CPL C  
JC addr
  - CLR C  
JC addr
  - SETB C  
JC addr
  - None of these
88. During the execution of MOV C, P3.0, would the bit value be taken from the input pin or from the output latch?
89. What would be the condition of the CY flag after execution of the JNC instruction?
90. How many instruction discussed in this chapter are capable of reading from input pins of a port, and not from its output latch?
91. Is there any bit-move instruction available in MCS-51 specifying bit addresses of both the source and destination?
92. How many bytes are necessary to accommodate CPL bit instruction?
93. How many bits of a 8051 device may be complemented by the CPL bit instruction?
94. Is it possible to implement the ORL bit instruction through the use of ANL bit and CPL bit instructions? Justify your answer.
95. What would happen if the second byte of the JC instruction is specified as FEH?
96. Is it possible to implement a NOR operation using MCS-51 instruction set for Boolean variables? If yes, then how would it be possible?
97. Why do some instructions read data from input pins and others from output latch in case of a directly addressed I/O port bit?
98. Which of the following instructions performs 16-bit increment?
- INC R0
  - INC R1
  - INC DPTR
  - None of these
99. If in Example 13.5, the second instruction of UPCLK routine is changed from ADD A, #01H to INC A, what would be the resulting change?

- (a) Overflow of minute counter
  - (b) DA A instruction cannot be used
  - (c) No change at all in performance
  - (d) None of these
100. Which of the following instructions communicates with the external data memory?
- (a) `MOVC A, @A + DPTR`
  - (b) `MOVX A, @R1`
  - (c) Either one
  - (d) None of these
101. `SWAP` instruction exchanges a pair of nibbles
- (a) Within the accumulator
  - (b) Between A and an indirectly addressed location
  - (c) Between A and a directly addressed location
  - (d) None of these
102. One-bit flag bits may be located within
- (a) Bit-addressable area
  - (b) Unused bits of PSW and also bit-addressable area
  - (c) Any unused data memory location
  - (d) None of these
103. Which of the following operations with two prime numbers would always generate another prime number?
- (a) Addition
  - (b) Multiplication
  - (c) Division
  - (d) None of these
104. If a table look-up procedure is adopted for 8-bit HEX to BCD conversion, then the length of the table would be
- (a) 10 bytes
  - (b) 100 bytes
  - (c) 250 bytes
  - (d) None of these
105. The minimum size of the stack for Example 13.2 program must be
- (a) 2 bytes
  - (b) 4 bytes
  - (c) 8 bytes
  - (d) None of these

## **Chapter FOUR—Assembly Programming**

1. Write a program to copy 16 bytes of data from the external data memory location 2000H onwards to internal data memory location 30H. Assume that port 1 is interfaced with the higher 8-bit address of the external data memory.
2. Sixteen-bit values of the square of integers are stored in a table that starts from program memory location 0200H onwards. The lower byte of the 16-bit number is at the lower address, and

the higher byte is at the higher address. Assuming that the accumulator contains the integer whose square is required, write a routine to get the result using table look-up procedure (MOVC instruction).

3. What are the conditions for matching two arrays?
4. Can a subroutine have more than one RET instruction?
5. Is it possible to generate prime numbers from 100 to 199 using 8051?
6. Write a program to convert any 8-bit binary number to its BCD equivalent.
7. Write a program to update the hour, minute and second counters of a RTC, assuming that all counters are in BCD and the display follows 12-h format.
8. Write a program to calculate the average of an array of unsigned positive integers. The array starts from 31H, and the number of terms in the array is available in location 30H. Store the calculated average in the location 2FH.
9. A random array of integers was generated and stored from location 31H onwards, storing its number of terms at location 30H. However, although the algorithm generally does not permit the repeat of any integer, to check this, develop a program ensuring that there is no repetition of any term. In case of repetition, the program should come out with CY flag as set; otherwise, CY flag should be cleared.
10. Develop a program to generate prime numbers by the method of divisions.

## **Chapter FIVE--- 8051 Interrupt system**

1. If all bits of SFR IP are cleared and INT0 and INT1 interrupts are received simultaneously, which one would be serviced first?
  - (a) INT0
  - (b) INT1
  - (c) Either of these
  - (d) None of these
2. An interrupt, like INT1, is enabled by setting
  - (a) IE.7
  - (b) IE.2
  - (c) both of these
  - (d) None of these
3. If any ISR is too long, its vector address must contain a
  - (a) CALL instruction
  - (b) JUMP instruction
  - (c) RETI instruction
  - (d) None of these
4. Any ISR must have at least
  - (a) one RETI instruction
  - (b) one RET instruction
  - (c) one RETI and one RET instruction
  - (d) None of these
5. INT0 input pin of 8051 is assigned to
  - (a) no other function

- (b) another function as P3.2
  - (c) two more function as P3.2 and T0
  - (d) None of these
6. What is the minimum duration for a low-level signal to be recognized as an interrupt?
    - (a) More than 1 cycle
    - (b) More than 2 cycles
    - (c) More than 3 cycles
    - (d) None of these
  7. What happens when TCON.1 is set by some software instruction?
    - (a) INT0 is acknowledged for a falling edge
    - (b) INT0 is disabled
    - (c) If it is enabled, then a software interrupt is generated
    - (d) None of these
  8. Which of the following interrupts is enabled immediately after a system reset?
    - (a) INT0
    - (b) INT1
    - (c) Either of these
    - (d) None of these
  9. Assuming that initially both interrupts were enabled, what would happen if, during execution of ISR of one interrupt, another interrupt signal interrupts the processor?
    - (a) ISR of other interrupt would be executed immediately
    - (b) If the later interrupt is of higher priority, then only its ISR would be executed, otherwise not
    - (c) The second interrupt ISR would be executed after completion of the RETI instruction of the first ISR and another instruction
    - (d) None of these
  10. What is meant by vectored interrupts?
  11. What is the purpose of TCON SFR?
  12. What is meant by falling-edge triggered?
  13. What happens if IE.7 is cleared?
  14. What are the characteristics of an ISR?
  15. Is it always necessary to assign a priority to an interrupt through IP SFR? Justify your answer?
  16. What alternative solution is available for a longer ISR?
  17. Why are multiple interrupts not generated by a low-level triggered signal even if it stays low for a longer duration than, say, 10 cycles?
  18. Is it possible to change the vector address of an interrupt by software commands or otherwise?
  19. What are the benefits of an interrupt?
  20. How would it be possible for 8051 to recognize a high-level interrupt?
  21. What are the general characteristics of any interrupt?
  22. What is the relation between an interrupt and a subroutine?
  23. If all interrupts have their default priorities, what is the purpose of providing IP SFR?
  24. How can we generate software interrupts in 8051?
  25. Why are accumulator and PSW saved before processing any interrupt?
  26. What precautions should we take to develop the ISR for a low-level triggered interrupt?



27. Is there any limitation about the length of an ISR?
28. In which condition may we need some extra hardware interfacing to deal with a low-level external interrupt signal?
29. Under which conditions may an ISR have multiple RETI instructions?

## **Chapter SIX--- 8051 Timer/Counter**

1. 8051/8052 Timers are capable of counting
  - (a) up
  - (b) down
  - (c) both (programmable)
  - (d) None of these
2. Timer/Counter configuration is selectable by
  - (a) hardware
  - (b) software
  - (c) either of these
  - (d) None of these
3. How many modes are offered by Timer 0?
  - (a) Two
  - (b) Three
  - (c) Four
  - (d) None of these
4. How many modes are offered by Timer 1?
  - (a) Two
  - (b) Three
  - (c) Four
  - (d) None of these
5. Setting TF0 bit of TCON by SETB instruction would
  - (a) generate a software interrupt
  - (b) nothing
  - (c) start reverse counting
  - (d) None of these
6. The source for counting of Timer 0 in its Counter mode would be
  - (a) P3.2 (INT0)
  - (b) P1.1
  - (c) P3.4 (T0)
  - (d) None of these
7. To which SFR does the RUN/STOP control bit TR0 for Timer 0 belong?
  - (a) TCON
  - (b) T2CON
  - (c) TMOD
  - (d) None of these
8. If Timer 0 is configured in Mode 3, then overflow for TH0 would set the bit, named
  - (a) TF0

- (b) TF1
  - (c) TL0
  - (d) None of these
9. The priority of Timer 2 is programmable through the SFR, named
- (a) T2CON
  - (b) RCAP2
  - (c) RCAP2H
  - (d) None of these
10. The three operating modes of Timer 2 are 16-bit auto-reload mode, 16-bit capture mode and
- (a) PWM mode
  - (b) baud-rate generator mode
  - (c) dual-timer mode
  - (d) None of these
11. What is the difference between a Timer and a Counter?
12. How is RUN/STOP control achieved in Timers 0 and 1?
13. How is RUN/STOP control achieved in Timers 2?
14. How does Timer 1 function in its Mode 3?
15. What is the relation between external crystal and Timer function as a Timer?
16. What is the role of IE register in Timer operations?
17. How can the priority of a Timer interrupt be changed?
18. Which of the processor resources is shared equally by all the three Timers?
19. What would happen if a Timer, say Timer 0 in Mode 1, is not stopped after its terminal counting and interrupt generation?
20. Is it possible to change the priority of a Timer during its run time?
21. What would happen if a Timer is started but its interrupt is not enabled?
22. Write a program to generate a square wave with 50% duty cycle using Timer 0. Assume the frequency to be 10 KHZ with the external crystal frequency of 12 MHZ.
23. Assume that both Timer 0 and Timer 1 are operating simultaneously. Develop suitable ISRs for these Timers so that during servicing of Timer 0, Timer 1 should not interrupt it and vice versa.

## **Chapter SEVEN--- 8051 Serial Communication**

1. Serial communication may be classified as
- (a) simplex, full-duplex and half-duplex
  - (b) synchronous and asynchronous
  - (c) either of these
  - (d) None of these
2. Serial data transmission is initiated by
- (a) placing the data byte in SBUF
  - (b) setting TI flag
  - (c) enabling Timer 1 interrupt
  - (d) None of these
3. If the logic level of a TxD line is high, it indicates
- (a) data bit or stop bit

- (b) data bit or stop bit or idle state
  - (c) stop bit or idle state
  - (d) None of these
4. Using one stop bit, if the baud rate is mentioned as, 9600, then the number of bytes transferred per second would be
- (a) 960
  - (b) 1067
  - (c) 1200
  - (d) None of these
5. For 9-bit transmission, the ninth bit is used as
- (a) stop bit
  - (b) multiprocessor communication
  - (c) parity bit
  - (d) None of these
6. To transmit the ninth bit, it should be placed in
- (a) bit 0 of next byte
  - (b) SMOD of PCON
  - (c) TB8 of SCON
  - (d) None of these
7. Which of the following bits, when set, would double the baud rate generated by Timer 1, except in Mode 0 of serial communication?
- (a) REN of SCON
  - (b) SMOD of PCON
  - (c) TF1 of TCON
  - (d) None of these
8. Serial data bits being received are initially stored in
- (a) temp. buffer
  - (b) accumulator
  - (c) SBUF
  - (d) None of these
9. If five 8051s are serially interfaced, which of the following serial communication mode would yield the best results?
- (a) mode 0
  - (b) mode 1
  - (c) mode 2
  - (d) None of these
10. For serial communication, standard frequency of the crystal for 8051 would be
- (a) 11.0592 MHZ
  - (b) 11.0952 MHZ
  - (c) 12 MHZ
  - (d) None of these
11. What is the format of serial communication of a byte of data?
12. Are start and stop bits always included for all modes of serial communication offered by 8051?
13. What is the purpose of REN bit in SCON SFR?

14. What is the difference between Mode 1 and Mode 3 of serial communication?
15. What is the utility of ninth bit?
16. How do we calculate the baud rate?
17. Which Timer is used for serial communication?
18. What is the purpose of Mode 0 of serial communication?
19. What role is played by SBUF in serial communication?
20. How is it possible to stop serial data reception in case of emergency?
21. How many types of serial communication are possible using 8051?
22. What would happen if serial data reception is going on, but data bytes are not being read from SBUF?
23. Is it possible to generate a baud rate of 75 using Timer 1 and 11.0592 MHZ crystal? If yes, then how? (Hint: Use Timer 1 in Mode 1).
24. Develop a method to receive continuous data from a temperature sensor in serial format.
25. Is it possible to use different baud rates for transmission and reception? If yes, then how?
26. A designed system of data acquisition using Mode 0 of serial communication is functioning perfectly. What would happen if the crystal of 8051 is changed from 12 to 11.0592 MHZ?
27. What purpose do the boosters serve in serial communication?
28. What is the maximum number of 8051 might be interlinked through serial transmission? Justify your answer.
29. Calculate the reload value for Timer 1 in Mode 2 to generate a baud rate of 2400, if 8051 is interfaced with a 12 MHZ crystal.
30. If the MSB of IE SFR ( $\overline{EA}$ ) is not set, would Timer 1 be able to generate the baud rate?

## Chapter EIGHT--- Interfacing: External Memory

1. Which of the following signals is used to generate the read strobe for external program memory, interfaced with MCS-51 devices?
  - (a)  $\overline{RD}$
  - (b)  $\overline{PSEN}$
  - (c)  $\overline{EA}$
  - (d) None of these
2. How many address signals are generated by MCS-51 to address external data memory, interfaced with it?
  - (a) 16
  - (b) 8
  - (c) 16 or 8
  - (d) None of these
3. Which of the following signals is used to latch the lower eight address bits from multiplexed lower address-data bus of MCS-51?
  - (a)  $\overline{RD}$
  - (b)  $\overline{PSEN}$
  - (c)  $\overline{EA}$
  - (d) None of these
4. Which ports of MCS-51 send out address signals to externally interfaced memory devices?

- (a) Ports 0 and 2
  - (b) Ports 1 and 3
  - (c) Ports 0 and 1
  - (d) None of these
5. Which of the following devices may be used to de-multiplex the lower address bus from multiplexed address-data bus of MCS-51?
- (a) 74373
  - (b) 74139
  - (c) 74138
  - (d) None of these
6. How chip select or chip-enable signals are generated for external memory devices interfaced with MCS-51?
- (a) By  $\overline{PSEN}$
  - (b) By unused addresses
  - (c) By unused port pins
  - (d) None of these
7. By which condition of the latching signal, the lower address signals of multiplexed address-data signals from MCS-51 are latched?
- (a) Rising edge
  - (b) Falling edge
  - (c) Either one
  - (d) None of these
8. The number of ALE signals per machine cycle for external data memory communication of MCS-51 would be
- (a) one
  - (b) two
  - (c) three
  - (d) None of these
9. The number of ALE signals per machine cycle for external program memory reading of MCS-51 would be
- (a) one
  - (b) two
  - (c) three
  - (d) None of these
10. In MCS-51, if only one lock bit is provided, then programming this lock bit would prevent
- (a) further programming
  - (b) access to on-chip program memory
  - (c) both of these
  - (d) None of these
11. Under which condition it may be necessary to interface external memory with MCS-51 devices?
12. What are the maximum size of program memory and data memory that may be interfaced with MCS-51?
13. How many signals are necessary for external memory for external memory interfacing with

MCS-51? From which ports are they generated? Are all of them alternate functions for these ports?

14. What are the differences between external program memory interfacing and external data memory interfacing with MCS-51?

15. What are the purpose of  $\overline{EA}$ ,  $\overline{PSEN}$  and ALE signals of MCS-51?

16. During one machine cycle of opcode-fetch, how many bytes are read from external program memory by MCS-51?

17. How many machine cycles are necessary for MOVX instruction to read a byte from external data memory?

18. What is the purpose of providing lock bits in MCS-51? What is the maximum number of lock bits provided?

19. Make a list of only those pin numbers which function differently in 6264 RAM and 2764 EPROM.

20. What type of communication takes place between MCS-51 and external program memory, synchronous or asynchronous?

21. Why MCS-51 is equipped with the  $\overline{PSEN}$  signal, in spite of the existence of a read signal available from the system?

22. Under which condition 8051 with internal 4K program memory would access external program memory?

23. Why it is not necessary to write 1s in Port 0 latch to read data from external RAM or ROM?

24. What is meant by 'Timing Diagram'?

25. Explain the technique of generating the *chip-select* signals for different memory devices.

26. Intel manufactured 8155 with RAM, I/O and Timer and 8755 with EPROM and I/O, to be interfaced with 8085 CPU. If these two devices are to be interfaced with MCS-51, is there any need of 74373? Justify your answer.

27. Design a circuit with 8052 Interfaced with an external 6264 RAM in such a manner so that the RAM may be used as data memory as well as program memory.

## Chapter NINE--- Interfacing: DAC/ADC

1. Which of the following techniques is used for DACs?

- (a) SAR
- (b) R-2R network
- (c) Both of these
- (d) None of these

2. Which of the following techniques is used for ADCs?

- (a) SAR
- (b) R-2R network
- (c) Both of these
- (d) None of these

3. Conversion time for DACs are generally in

- (a) milliseconds
- (b) microseconds
- (c) nanoseconds

- (d) None of these
4. For any ADC built around successive approximation technique, which of the following is essential?
- (a) DAC
  - (b) Comparator
  - (c) Both of these
  - (d) None of these
5. Which type of logic is used in ADCs?
- (a) Sequential
  - (b) Combinational
  - (c) Both of these
  - (d) None of these
6. How many 8-bit ports are necessary to interface an 8-bit ADC?
- (a) One
  - (b) Two
  - (c) Three
  - (d) None of these
7. For National 0809 ADC, which of the following signals indicate that converted data is ready and available?
- (a) ALE
  - (b) OE
  - (c) START
  - (d) None of these
8. To convert only one analog channel continuously, which of the following technique may be adopted for 0809 ADC?
- (a) Connect ALE with START
  - (b) Connect EOC with START
  - (c) Connect OE with START
  - (d) None of these
9. What would be the frequency of a square wave if both its on-time and off-time are 25 microseconds?
- (a) 200 Hz
  - (b) 2 KHz
  - (c) 200 KHz
  - (d) None of these
10. How many I/O lines are necessary to interface a 12-bit DAC with 8051?
11. How the end of conversion signal is generated for an ADC using successive approximation technique?
12. If all three channel select lines (A, B and C) are connected with Vcc, which channel's analog input would be digitized by 0809 ADC?
13. What is the purpose of a Sample and Hold unit? When and where it is to be interfaced?
14. How the duty cycle of a square wave may be changed to 75 per cent?
15. How can the flash-converter type ADC convert any analog signal to its digital form almost instantly?

16. What do we achieve by connecting START and ALE for ADC 0809?
17. ADC 0809 is capable to convert any analog signal between 0V and 5V. How it may be used to convert an analog signal between -1V and 1V?
18. What would happen if the converted data is not read till the next conversion-over signal?
19. Which type of waveform is to be input to the DAC of a SAR type ADC if the ADC is to convert an analog signal like a sine wave?
20. Does an ADC take same time to convert analog signals of different magnitudes?

## **Chapter TEN---Interfacing: Keyboards/ Display Devices**

1. If decremented by DJNZ instruction, which of the following initial counter values would generate maximum delay?
  - (a) #0FFH
  - (b) #00H
  - (c) #60H
  - (d) None of these
2. Membrane type of keys are activated through
  - (a) mechanical contact
  - (b) capacitance
  - (c) induction
  - (d) None of these
3. Any mechanical contact type key can produce a maximum of
  - (a) one state
  - (b) two states
  - (c) three states
  - (d) None of these
4. To input logic 'low' to any input pin of a port, the relevant circuit should be able to
  - (a) sink current
  - (b) produce 0V
  - (c) both of these
  - (d) None of these
5. Bouncing of any mechanical contact type key may last for a maximum of
  - (a) 40 microseconds
  - (b) 4 milliseconds
  - (c) 1/4 of a second
  - (d) None of these
6. For hardware debouncing, the key with pull-up resistor should be attached with
  - (a) another resistor
  - (b) a capacitor
  - (c) a diode
  - (d) None of these
7. For software debouncing, it is to be ensured that the key is
  - (a) released
  - (b) sensed for more than 40 milliseconds



- (c) sensed twice
  - (d) None of these
8. The maximum number of keys may be interfaced with seven Port pins would be
- (a) 7
  - (b) 10
  - (c) 12
  - (d) None of these
9. To read any two-dimensional keyboard matrix, the output pins should output
- (a) one 0 and others 1
  - (b) one 1 and others 0
  - (c) either of these
  - (d) None of these
10. If more than one key is passed, then the routine KSCAN would return
- (a) first scanned key
  - (b) last scanned key
  - (c) no key
  - (d) None of these
11. How do the Hall-effect keys function?
12. Are springs essential for mechanical contact type keys?
13. What are the essential features of interfacing a mechanical contact type key with a port pin of any microcontroller?
14. What is bouncing? Is it applicable for all types of keys? How can any key be debounced?
15. What is the difference between hardware debouncing and software debouncing?
16. What are the limitations of one-dimensional array of keys?
17. What are the advantages of a two-dimensional array of keys?
18. What is the methodology of scanning a two-dimensional keyboard?
19. What is the role of a debounce counter in any key scanning routine?
20. What would happen if the DELAY routine is not used in the routine SCAN1?
21. What is the difference between tactile keys and membrane type keys?
22. When we should interface one key per input pin, and when we should interface multiple keys per input pin?
23. Under which conditions hardware debouncing would be more acceptable than software debouncing? (Hint: RESET)
24. What purpose does a key counter serve in any two-dimensional key releasing?
25. How is it possible to generate two difference codes for key pressing and key releasing?
26. If a 8051 microcontroller is used to read a keyboard and communicate with host computer through serial interface, what is the maximum number of keys may be interfaced in the keyboard?
27. What would happen if in routine SCAN, register R6 is loaded by #80H instead of #7FH?
28. Is it possible to rewrite SCAN1 routine without using R0?
29. When viewed from top, the cathode side of a cylindrical LED is
- (a) circular
  - (b) flat
  - (c) either of these
  - (d) None of these

30. LEDs are capable of displaying
- (a) one state
  - (b) two states
  - (c) three states
  - (d) None of these
31. LEDs should be used with
- (a) nothing
  - (b) a resistor in parallel
  - (c) a resistor in series
  - (d) None of these
32. Seven-segment displays are available as
- (a) common anode
  - (b) common cathode
  - (c) both of these
  - (d) None of these
33. In multiplexed display scheme with seven-segment display,
- (a) only one digit is driven at a time
  - (b) only one segment is driven at a time
  - (c) only one segment of only one digit is driven at a time
  - (d) None of these
34. Generally, in multiplexed display scheme, all digits are refreshed
- (a) once in a second
  - (b) 10 times a second
  - (c) 100 times a second
  - (d) None of these
35. To drive a 12-digit multiplexed seven-segment display, the number of port pins for segment drive would be
- (a) 8
  - (b) 12
  - (c) 16
  - (d) None of these
36. In general, multiplexed seven-segment display scheme is adopted to
- (a) save space
  - (b) save power
  - (c) brighten the display
  - (d) None of these
37. How many varieties of LEDs are commercially available?
38. Why a resistor in series is always necessary to interface any LED?
39. Why a driver is necessary if an LED is to be driven by logic 1?
40. What is the difference between common anode and common cathode type of seven-segment display?
41. Why a digit is to be converted to its display pattern before display?
42. How are seven-segment display multiplexed?
43. Why a delay routine is necessary for software for refreshing multiplexed display?

44. How interrupts may be used for multiplexed seven-segment display digits?
45. How is economy achieved by interfacing keyboard and display simultaneously?
46. Is it possible to use a decoder, like 74138, as digit driver?
  
47. Why LEDs should never be used to replace diodes?
48. Make two lists of electronic devices using LEDs and seven-segment displays.
49. Like seven-segment displays, which types of LEDs are available in common anode and common cathode configurations?
50. Apart from displaying numerical values, can seven-segment displays be used for displaying English alphabets?
51. Interface with 8051 one key and one LED. Develop a program so that whenever the key is pressed, the LED would be turned on. The LED may be turned off by releasing the key.
52. In spite of being composed of eight LEDs, why the device is known as seven-segment display?